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"Atomistic" Simulation of Decanano Devices

A. Asenov
A. R. Brown, J. H. Davies, S. Kaya, G. Slavcheva
Department of Electronics and Electrical Engineering
University *of* Glasgow

S. Saini
NASA Ames Research Centre

Summary

- Introduction
- Random Dopant Fluctuations
- Single Charge Trapping
- Oxide Thickness Fluctuations
- Conclusions

Scaling of MOSFETs to decanano dimensions

(International Roadmap for Semiconductors - 1999 Edition)

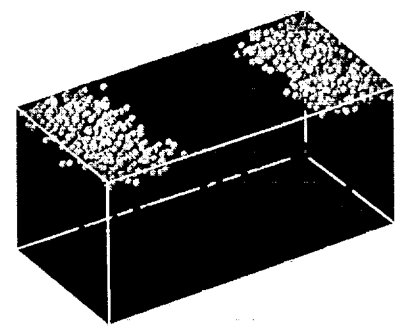
Year	1999	2001	2004	2008	2011	2014
MPU Gate Length *(nm)*	140	100	70			
Oxide thickness *(nm)*	1.9-2.5	1.5-1.9	1.2-1.5			
Drain extensions *(nm)*	42-70	30-50				

Solution exists

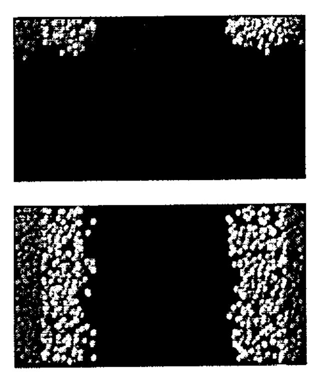
Solution Being Pursued

No Known Solutions

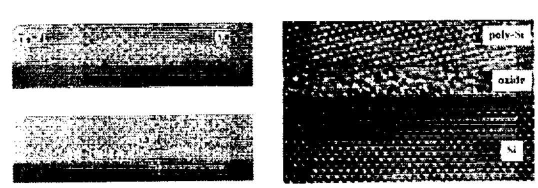
'True' dopant distribution in a 50x50 nm MOSFET



'True' dopant distribution in a 50x50 nm MOSFET



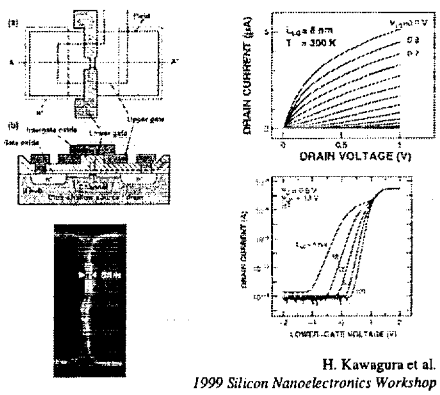
TEM view of ultrathin gate oxides



H.S. Momose et al.
IEEE Trans. Electron Dev.
45 691 (1998)

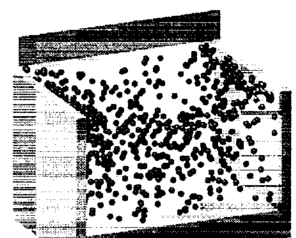
A. Chin et al.
IEEE Electron Dev. Lett.
18 417 (1997)

MOSFET with 8 nm gate length



H. Kawagura et al.
1999 Silicon Nanoelectronics Workshop

Solution domain in 3D 'atomistic' simulation



50×50 nm MOSFET

- ❑ 3D drift-diffusion simulations
- ❑ Fine grain discretisation
- ❑ Statistical ensembles of microscopically different devices
- ❑ Estimation of averages and standard deviations

Summary

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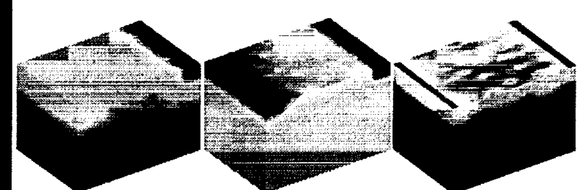
- ❑ Conclusions

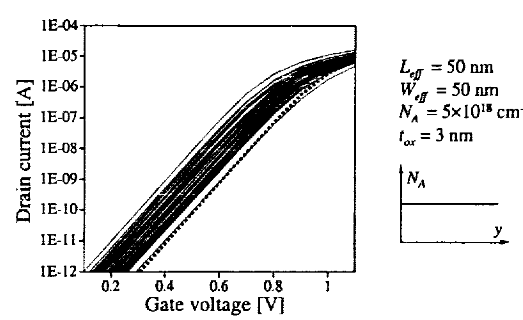
Typical results of 3D 'atomistic' simulation for a 50×50 nm MOSFET



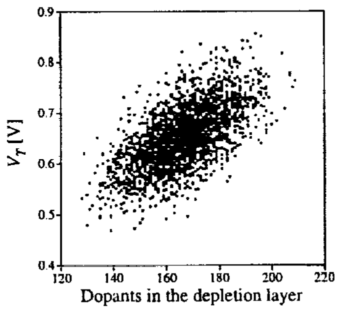
Potential distribution | Electron concentration | Current density

- ❑ Random Dopant Fluctuations
  - Simulation approach
  - Fluctuation resistant architectures
  - The effect of the poly-Si gate
  - Quantum corrections

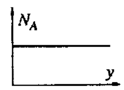
I-V characteristics of an ensemble of 50 microscopically different Devices



Threshold voltage vs. number of dopants in the gate depletion region



L_{eff} = 50 nm
W_{eff} = 50 nm
N_A = 5×10^{18} cm^{-3}
t_{ox} = 3 nm



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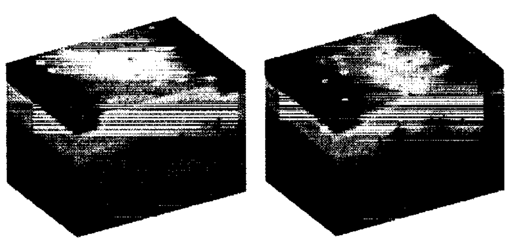
Potential distribution in two microscopically different 50×50 nm MOSFETs



V_T = 0.55 V

V_T = 0.78 V

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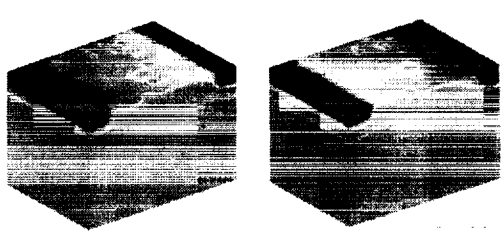
Threshold voltage asymmetry in a 50×50 nm MOSFET



V_T = 0.67 V

V_T = 0.80 V

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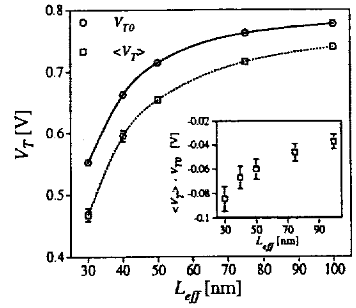
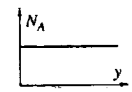
Threshold voltage and threshold voltage lowering as a function of the channel length



W_{eff} = 50 nm
N_A = 5×10^{18} cm^{-3}
t_{ox} = 3 nm



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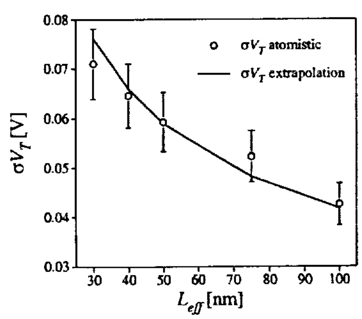
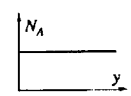
Standard deviation in the threshold voltage as a function of the effective channel length



W_{eff} = 50 nm
N_A = 5×10^{18} cm^{-3}
t_{ox} = 3 nm



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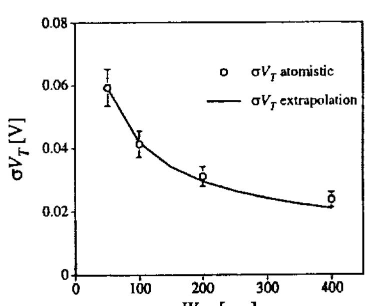
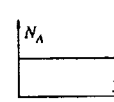
Standard deviation in the threshold voltage as a function of the effective channel width



L_{eff} = 50 nm
N_A = 5×10^{18} cm^{-3}
t_{ox} = 3 nm



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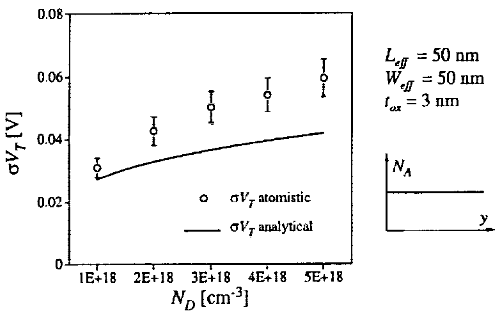
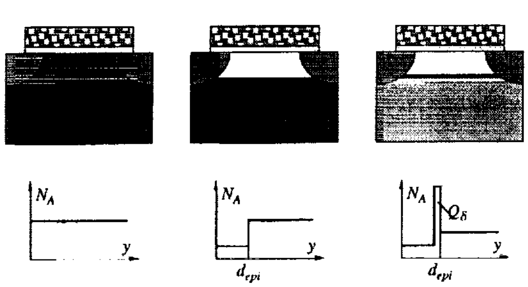
Standard deviation in the threshold voltage as a function of the doping concentration



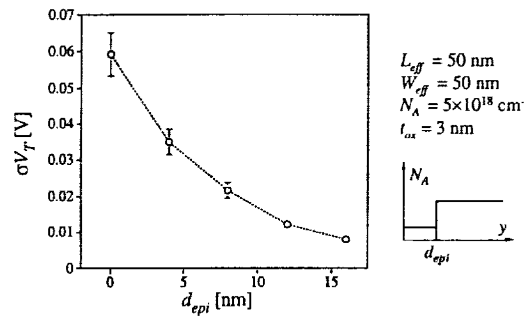
❑ Random Dopant Fluctuations

- Simulation approach
- Fluctuation resistant architectures
- The effect of the poly-Si gate
- Quantum corrections

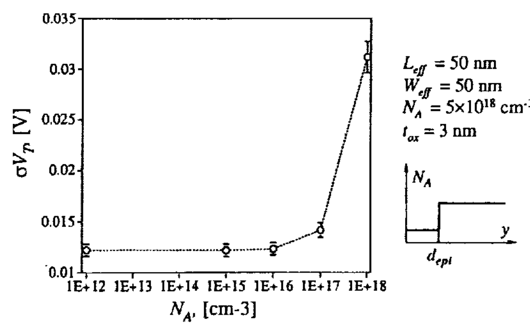
Random dopant resistant MOSFET architectures



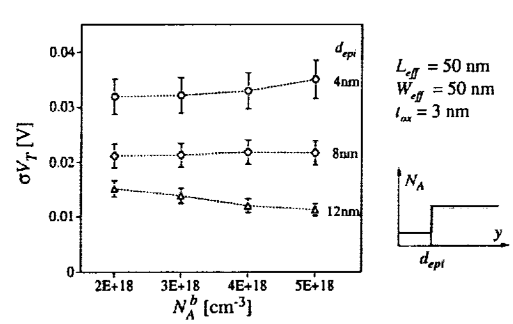
Standard deviation in the threshold voltage as a function of the thickness of the epitaxial undoped channel layer



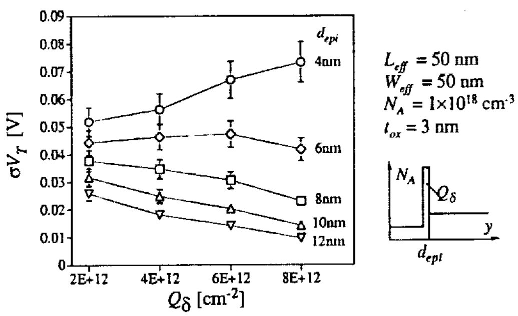
Standard deviation in the threshold voltage as a function of the doping concentration in the epitaxial channel



Standard deviation in the threshold voltage as a function of the doping concentration behind the epitaxial channel



Standard deviation in the threshold voltage as a function of the δ-doping concentration Q_δ in epitaxial δ-doped MOSFETs



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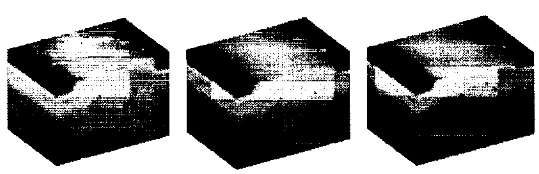
Potential distribution



Uniform doping | Epitaxial channel | Epitaxial channel + delta doping

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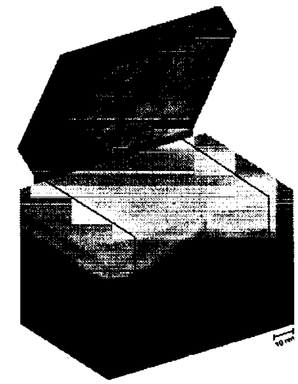
Potential distribution at the Si/SiO_2 interface and the Poly-Si/ SiO_2 interface



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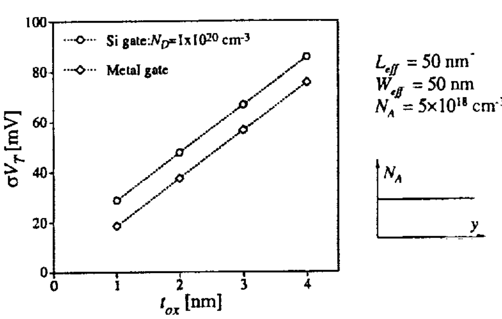
Dependence of σV_T on the oxide thickness t_{ox} for single crystal silicon gate and metal gate MOSFETs



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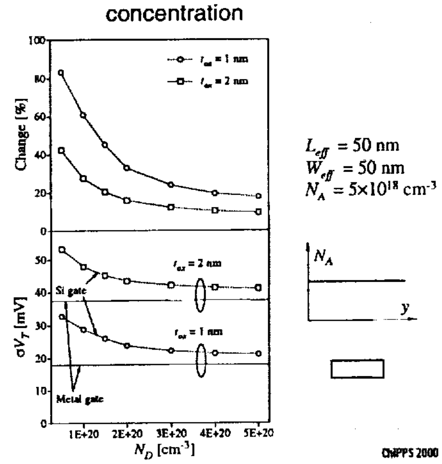
Dependence of σV_T on the gate doping concentration



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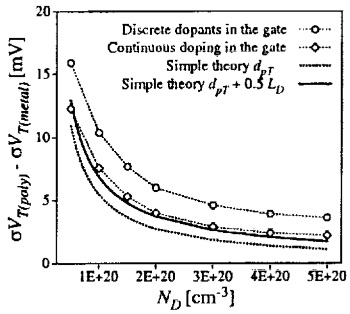
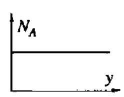
Increase in the threshold voltage standard deviation associated with the single crystal silicon gate



L_{eff} = 50 nm
W_{eff} = 50 nm
N_A = 5x10^{18} cm^{-3}
t_{ox} = 3 nm



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The density gradient approach
(at low drain voltage)

❑ Solve self-consistently

$$\nabla.(\varepsilon\nabla\psi) = -q\left(p - n + N_D^+ - N_A^-\right)$$

$$2b_b \frac{\nabla^2\sqrt{n}}{\sqrt{n}} = \phi_n - \psi + \frac{kT}{q}\ln\frac{n}{n_i}$$

❑ Solve

$$\nabla.\mu_n n\nabla V = 0$$

to extract the current

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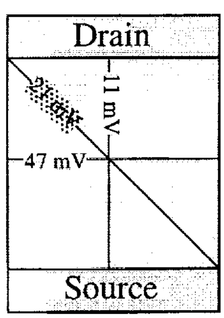
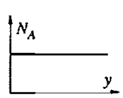
Effect of the poly-Si gate grain boundaries on the threshold voltage



L_{eff} = 50 nm
W_{eff} = 50 nm
N_A = 5x10^{18} cm^{-3}
t_{ox} = 3 nm



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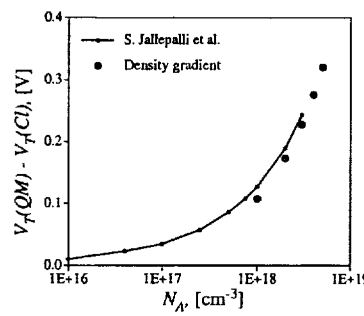
Quantum mechanical threshold voltage shift as a function of the doping concentration



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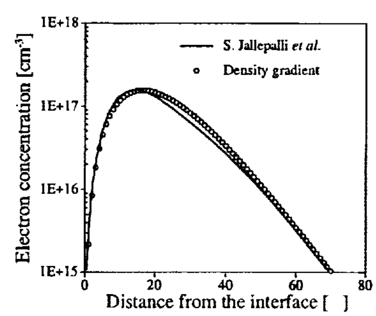
Quantum mechanical charge distribution in the inversion layer



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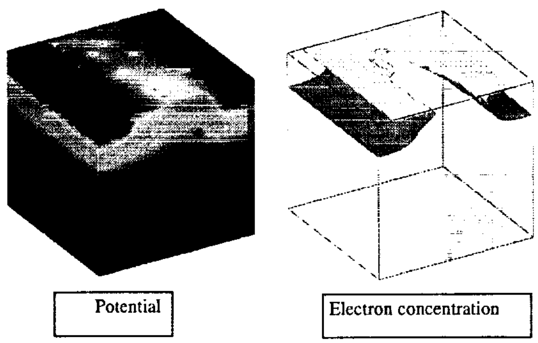
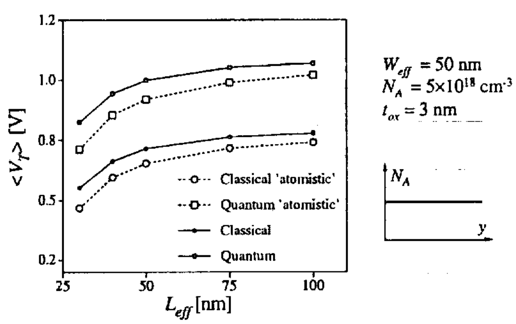
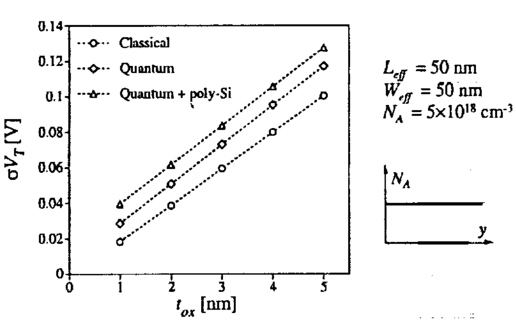
Potential and electron distribution in a 30×50 nm MOSFETs



Average threshold voltage as a function of the gate length in 50 nm wide MOSFETs



Threshold voltage lowering as a function of the gate length in 50×50 nm MOSFETs



Summary

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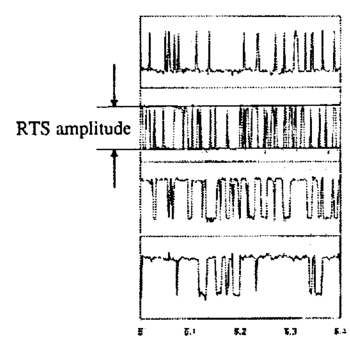
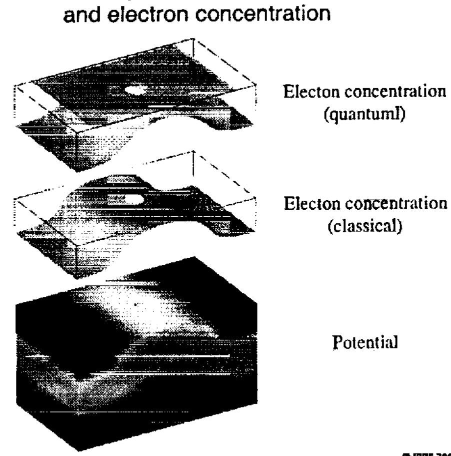
Random telegraph signal in a 0.15×0.97 μm^2 MOSFET

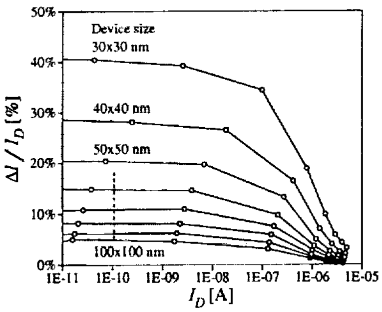


Z. Çelik-Butler et al.
IEEE TED 47 646 (2000)

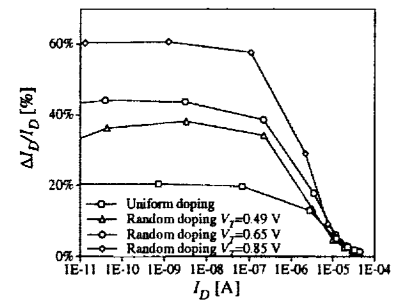
The effect of a single electron trapping on potential and electron concentration



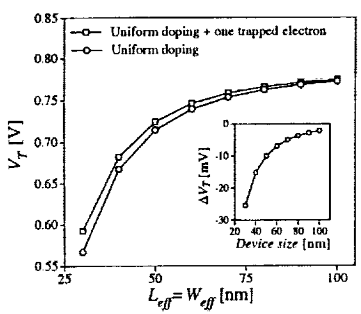
Relative RTS amplitude as a function of the drain current for a set of square MOSFETs



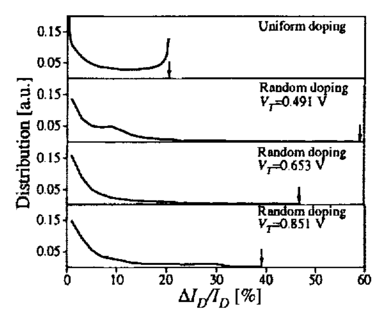
Drain current dependence of the highest RTS amplitudes in a 50×50 nm MOSFET with continuous doping and random discrete dopants



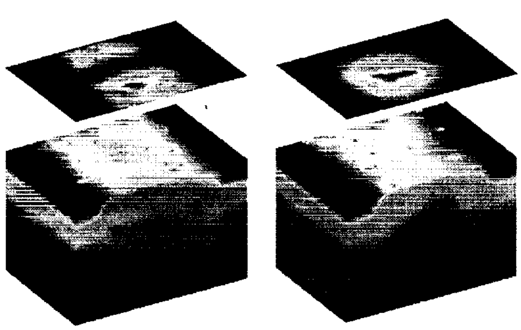
Effect of single electron trapping on the threshold voltage in decanano MOSFETs with square geometry



Distribution of the RTS amplitudes in a 50×50 nm MOSFET with continuous doping and random discrete dopants



Potential distributions in a 50×50 nm MOSFETs (bottom). Magnitude of the RTS amplitude associated with a single electron trapping (top).



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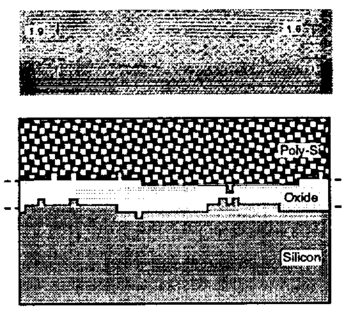
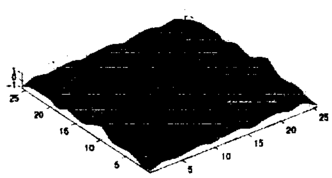
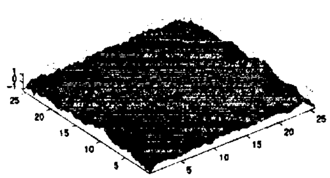
Thickness fluctuations of ultrathin gate oxides

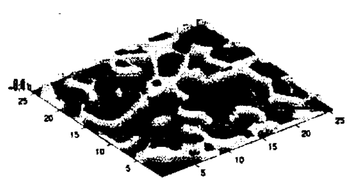


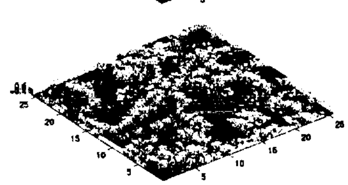
Reconstruction of the Si/SiO_2 interface topology



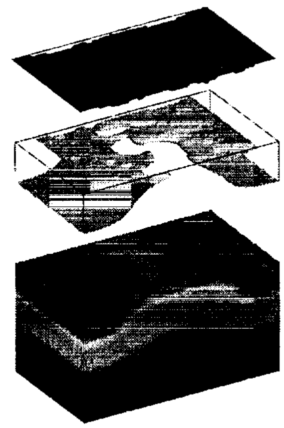


Digitisation of the Si/SiO_2 interface topology

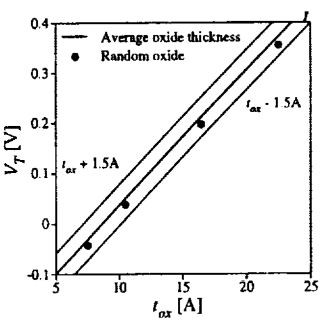




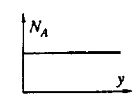
Simulation of oxide thickness fluctuation effects



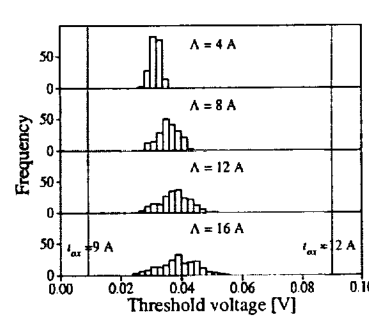
Average threshold voltage as a function of the average oxide thickness in a 30×30 nm MOSFET



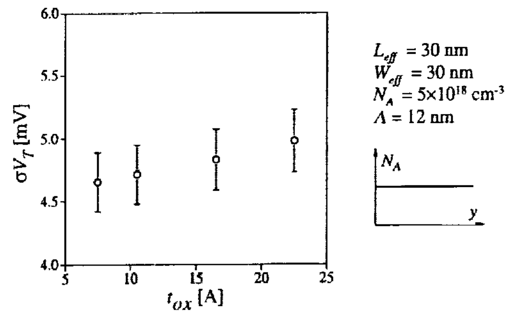
L_{eff} = 30 nm
W_{eff} = 30 nm
N_A = 5×10^{18} cm^{-3}
Λ = 12 nm



Threshold voltage distributions for different correlation lengths



Threshold voltage standard deviation as a function of the oxide thickness



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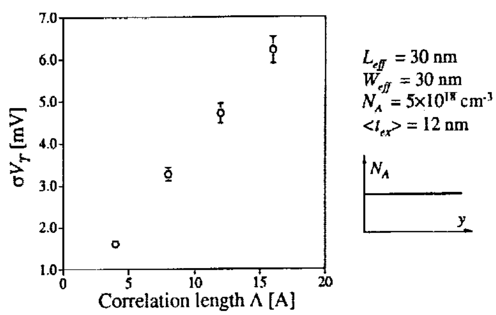
Threshold voltage standard deviation as a function of the correlation length



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Conclusions

- When the devices are scaled to decanano dimensions the discreteness of charge and matter introduces significant 'intrinsic' parameter fluctuations.
- Atomic level 3D process and device modelling on statistical scale is required to understand the effects, the scale of the fluctuations and to design fluctuation resistant devices.

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